WHAT IS CLAIMED IS:

1. A method for reducing power consumption of an integrated circuit device, comprising:

receiving a command issued to the device;

receiving an input signal by a latch circuit in conjunction with the command;

determining if the command is an invalid command; and

latching the first input signal with the latch circuit only if it is determined the command is not invalid.

2. The method of claim 1, wherein determining if the command is an invalid command comprises determining NOP (no operation) and DIS (device deselect) commands are invalid commands.

3. The method of claim 1, wherein the device is a memory device and the latch circuit is an address latch circuit.

4. The method of claim 1, wherein latching the input signal with the latch circuit comprises asserting a latch control signal.

5. The method of claim 4, further comprising preventing the latch circuit from latching the input signal in response to determining the command is invalid by de-asserting the latch control signal.

6. The method of claim 5, wherein de-asserting the latch control signal comprises generating an invalid command signal in response to determining the command is invalid.

7. An integrated circuit device, comprising:

a command interface for receiving commands issued to the device;

one or more latch circuits for receiving input signals in conjunction with corresponding commands received by the interface; and

control circuitry configured to determine if the corresponding commands are valid and generate one or more latch control signals to cause the latch circuits to latch the input signals only if the corresponding commands are valid.

8. The device of claim 7, wherein the input signals comprise address signals.

9. The device of claim 7, wherein the input signals comprise one or more command signals.

10. The device of claim 7, wherein the latch circuits comprise:

an input for receiving an input signal;

at least two stages of cross-coupled inverters;

a first switch configured to couple the input to the first stage when a latch control signal is at a first logic state and to decouple the input from the first stage when the latch control signal is at a second logic state; and

a second switch configured to couple an output of the first stage to the second stage when the latch control signal is at the second logic state and to decouple the second stage from the first stage when the latch control signal is at the first logic state.

11. The device of claim 10, wherein the control circuitry is configured to place or maintain the latch control signal in the first logic stage when an invalid command is detected.

12. The device of claim 7, wherein the command interface comprises a command bus to receive one or more command signals.

13. The device of claim 12, wherein the control circuitry comprises detection circuitry to decode the command signals and generate an invalid command signal in response to detecting a command considered invalid.

14. A memory device, comprising:

one or more address receivers for receiving address signals driven on an external address bus in conjunction with commands issued to the device;

one or more address latch circuits for latching address signals received by the address receivers and supplying address signals to corresponding output drivers;

control circuitry configured to generate at least one latch control signal to cause the address latch circuits to supply first address signals to the corresponding output drivers if corresponding first commands are valid; and

an invalid command detector to generate a signal to inhibit the latch control signal to prevent the address latch circuits from supplying second address signals to the corresponding output drivers if corresponding second commands are invalid.

15. The device of claim 14, wherein the memory device further comprises one or more command latch circuits for latching command signals responsive to the latch control signal generated by the control circuitry.

16. The device of claim 14, wherein the invalid command detector receives, as in input, a chip select signal.

17. The device of claim 14, wherein the address latch circuits comprise:

at least two stages of cross-coupled inverters;

a first switch configured to couple an output of an address receiver to the first stage when the latch control signal is at a first logic state and to decouple the output of the address receiver from the first stage when the latch control signal is at a second logic state; and

a second switch configured to couple an output of the first stage to the second stage when the latch control signal is at the second logic state and to decouple the second stage from the first stage when the latch control signal is at the first logic state.

18. The device of claim 17, wherein the control circuitry is configured to place or maintain the latch control signal in the first logic stage when an invalid command signal is asserted by the invalid command detector.

19. The device of claim 18, wherein the control circuitry comprises a switch controlled by the invalid command signal.

20. The device of claim 18, wherein the invalid command detector asserts the invalid command signal in response to detecting at least one of a NOP (no operation) command and a DIS (device deselect) command.